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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,371	JOHNSON, LEITH	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *24 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendment and Remarks filed on August 16, 2005 regarding application 10/017,371 filed on December 7, 2001.

2. Claims 1-26 are pending in the application under consideration.

Claims 2, 9, 15, 19, 23 and 25 have been amended.

Claims 24 and 26 have been canceled.

3. ***Response to Remarks and Amendments***

Applicants' remarks and amendments have been fully and carefully considered with examiner's response set forth below.

As to remark for claim 1:

Applicant contends that the prior art (Gulick et al., US 6,314,501) fails to teach the limitation of "wherein the plurality of physical resources identifiers are numbered sequentially beginning with zero" because of the memory holes (high memory hole and low memory hole) shown in figure 5 of Gulick et al.. The examiner disagrees with this assessment.

It should be noted that the "low/high memory hole," just like "low/high memory window" and "shared memory window," are **physical resources identifiers** referring to different segments of the overall memory space. They are allocated sequentially, one next to the other, beginning from address zero, as illustrated in figure 5. The name of "memory hole" in no way implies that the particular memory segment is totally "blank" and does not store any information. As applicant admits and correctly points out, the "high memory hole" is assigned to an I/O device and the "low memory hole" is also

assigned to an I/O device. Even though they are unavailable for storing data or instructions, they are used by I/O devices to store information related to their respective I/O operations. Hence the "low/high memory hole," just like "low/high memory window" and "shared memory window," are useful, physical resources as far as the system operations are concerned.

Further, figure 5 also shows a memory allocation of the MSU memory space (504), which is another example of a "plurality of physical resources identifiers are numbered sequentially beginning with zero," which comprising **physical resources identifiers** of "low memory," "high memory" and "shared memory" without any "memory hole."

Therefore, the examiner's position regarding the patentability of claims 1, and those claims dependent from them, remains the same as stated in the previous Office Action.

As to remark for claim 24:

Applicant contends that the prior art (Gulick et al., US 6,314,501) fails to teach the limitation of claim 24, which recites "copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses." The examiner disagrees with this assessment.

In addition to the explanation provided by the examiner in the previous Office Action regarding this feature [an operating system can directly read from another operating system's memory page. Also, one operating system instance can load data (i.e., copy from the first subset) destined for another operating system directly into the

other operating system's data area (i.e., the second subset) (column 15, lines 47-52)], many other instances also exist in the disclosure by Gulick et al. For example, figure 3 shows that the contents of the "shared memory" of the OS#4 DRAM memory are copied to the "shared memory" segment of the MSU memory space (350). Other examples illustrating the "copying" from one memory address to a second memory space can be found in figures 4, 5, 10, 11, and 12.

Therefore, the examiner's position regarding the patentability of claim 24, which has been canceled but the original feature incorporated into claims 23 and 25, remains the same as stated in the previous Office Action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5, 7-11, 13-21, and 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Gulick et al. (US 6,314,501).

As to claim 1, Gulick et al. disclose **in a partitionable computer system** [Computer System and method for Operating Multiple Operating systems in Different partitions of the Computer System and for Allowing the Different Partitions to Communicate with One Another through Shared Memory (title)] **including a plurality**

of machine resources having a plurality of machine resource identifiers [the corresponding a plurality of machine resources is the plurality of memory storage unit (figure 2, 220A~220D) which form the main memory (figure 1, 160) of the computer system (figure 1, 100). Each one of the plurality of Memory Storage Unit (MSU) has its own address space (i.e., the identifier) as shown in figure 3], **a method for creating a physical resource identifier space in a partition of the partitionable computer system** [figure 3 shows a plurality of partitions and how their physical address spaces are related to the MSU address space], **the method comprising steps of**:

(A) **establishing a mapping** [figure 3 shows the address mapping between 4 instances of partitions and a MSU] **between a plurality of physical resource identifiers** [figure 3 shows 4 instances of partitions and their associated physical resource identifiers] **and at least some of the plurality of machine resource identifiers** [figure 3 also shows the machine resource associated with the MSU], **wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero** [the address space of each of the partition always begins at address zero (column 14, lines 48-67); figure 5]; **and**

(B) **providing**, **to a software program executing in the partition** [the operating system (column 14, lines 48-67); figure 3], **an interface for accessing the at least some of the plurality of machine resources using the plurality of physical resource identifiers** [figures 4 and 5; column 16, lines 30-67].

As to claim 2, Gulick et al. disclose that **the plurality of machine resources** [the corresponding a plurality of machine resources is the plurality of memory storage unit

(figure 2, 220A~220D) which form the main memory (figure 1, 160) of the computer system (figure 1, 100)] **comprises a plurality of machine memory locations** [figures 3 and 5 show the MSU memory space; figure 7 shows the case of multiple MSUs], **wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses** [figures 5, 6, and 7], **and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses** [figure 5 shows 3 instances of partitions and their associated physical address space].

As to claim 3, Gulick et al. disclose that **the method of claim 1 further comprising a step of performing the steps (A) and (B) for each of a plurality of partitions of the partitionable computer** [figure 5 shows that steps (A) and (B) are performed for all 3 partitions.

As to claim 4, Gulick et al. disclose that **the step (A) comprises a step of creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers** [figures 4 and 5; Each TCT 270 performs address relocation, reclamation, and translation for memory addresses issued by the processors to which it is connected, as described more fully below (column 11, lines 51-54); column 22, lines 9-67].

As to claim 5, Gulick et al. disclose that **the interface comprises means for translating a physical resource identifier selected from among the plurality of**

physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping [figures 4 and 5; column 22, lines 9-67].

As to claim 7, Gulick et al. disclose that **the software program comprises an operating system** [figure 3 shows that the software program executing in each of the 4 partitions is an operating system].

As to claim 8, refer to "As to claim 1."

As to claim 9, refer to "As to claim 2."

As to claim 10, refer to "As to claim 4."

As to claim 11, refer to "As to claim 5."

As to claim 13, refer to "As to claim 7."

As to claim 14, refer to "As to claim 1" through "As to claim 5." Further, Gulick et al. disclose that [The TCT 270 takes a processor's memory read/write address (after any relocation and/or reclamation) and passes it through an address translation function (column 23, lines 7-23). Hence, the desired data resides in the machine resource is accessed for read or write operations using the translated address].

As to claim 15, refer to "As to claim 2."

As to claims 16-17, Gulick et al. disclose that [The TCT 270 takes a processor's memory read/write address (after any relocation and/or reclamation) and passes it through an address translation function (column 23, lines 7-23). Hence, the desired data resides in the machine resource is accessed for read or write operations using the translated address].

As to claim 18, refer to "As to claim 14."

As to claim 19, refer to "As to claim 2."

As to claims 20-21, refer to "As to claims 16-17."

As to claim 23, refer to "As to claim 1" through "As to claim 5." Further, figures 10, 11, and 12 show the address remapping between a subset of plurality of memory locations (showing OS#1, OS#2, and OS#3) to a subset of a plurality of machine memory address (MSU memory space) without rebooting the computer system (column 5, lines 46-67). This is achieved by relocation (column 16, lines 18-29) and reclamation (column 16, lines 30-50).

Further, Gulick et al. teach **copying the contents of the first subset of the plurality of machine memory addresses to the second subset of the plurality of machine memory addresses** [an operating system can directly read from another operating system's memory page. Also, one operating system instance can load data (i.e., copy from the first subset) destined for another operating system directly into the other operating system's data area (i.e., the second subset) (column 15, lines 47-52)]. Moreover, Gulick et al. show in figure 3 that the contents of the "shared memory" of the OS#4 DRAM memory are copied to the "shared memory" segment of the MSU memory space (350). Other examples illustrating the "copying" from one memory address to a second memory space can be found in figures 4, 5, 10, 11, and 12.

As to claim 25, refer to "As to claim 23."

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick et al. (US 6,314,501).

With respect to claims 6, 12 and 22, Gulick et al. do not teach that **the interface comprises a Content Addressable Memory that establishes the mapping**. However, the subject matter of content addressable memory is well known and is widely adopted in a computer system to reduce memory access latency and to increase operational speed (see Microsoft Computer Dictionary, 5th edition, Microsoft Press, 2002, page 125 – content-addressed storage). Therefore, it would be obvious for ones of ordinary skills in the art at the time of Applicant's invention to recognize the benefit offered by a content addressable memory and to incorporate it into the existing apparatus disclosed by Gulick et al. to further enhance the performance of the system.

8. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Kirk, (US 5,875,464), "Computer System with Private and Shared partition in Cache."
- Van Doren, (US Patent Application Publication 2001/0037435), "Distributed Address Mapping and Routing Table Mechanism That Supports Flexible

Configuration and Partitioning in a Modular Switch-Based Shared-memory Multiprocessor Computer System."

- Chi et al., (US 5,940,870), "Address Translation for Shared-memory Multiprocessor Clustering."
- Greenstein et al., (US 5,784,702), "System and method for Dynamically Performing Resource Reconfiguration in a Logically Partitioned Data Processing System."
- White et al., (US 5,721,858), "Virtual Memory Mapping Method and System for memory Management of pools of Logical Partitions for BAT and TLB Entries in a Data Processing System."
- Huber et al., (US 5,455,775), "Computer Design System for Mapping a Logical Hierarchy into a Physical Hierarchy."
- Parrish et al., (US 5,117,350), "Memory Address Mechanism in a Distributed memory Architecture."
- George et al., (US 4,51,964), "Dynamic Physical Memory Mapping and Management of Independent Programming Environments."
- Alvarez et al., (US 3,723,976), "Memory system with Logical and Real Addressing."

Conclusion

9. Claims 1-23 and 25 are rejected as explained above.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner

PIERRE BATAILLE
PRIMARY EXAMINER
9/5/05